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09/936,267	09/10/2001	Masatoshi Ishikawa	110602	2617

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EXAMINER	
MISLEH, JUSTIN P	
ART UNIT	**PAPER NUMBER**
2612	7

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/936,267	Applicant(s) ISHIKAWA ET AL.	
	Examiner Justin P Misleh	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 7 is/are allowed.

6)☒ Claim(s) 1 and 6 is/are rejected.

7)☒ Claim(s) 2 - 5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 September 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The disclosure is objected to because of the following informalities: misplacement of reference sign description.

Reference sign 1000 is first described in connection with figure 3; however, reference sign 1000 is first shown in figure 1.

Appropriate correction is required.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors, including possible errors similar to one detailed above and below with respect to the detailed description and the drawings. **Applicant's cooperation is requested in correcting any errors of which Applicant may become aware in the specification and/or drawings.**

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 170i and 180j.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the Examiner does not accept the changes, Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

5. The information disclosure statements (IDS) submitted on 10 September 2001 and on 20 December 2001 were filed before the mailing date of this Non-Final Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner is considering the information disclosure statements.

Double Patenting

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. **Claims 1 and 6** (herein referred to as: App. Claims 1 and 6) is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claim 1 of U.S. Patent No. 6,608,296 B1 (herein referred to as: Patent Claim 1) in view of Akerib.

8. For **Claims 1 and 6**, Patent Claim 1 and App. Claims 1 and 6 both provide the following limitations: A high-speed vision sensor, comprising:

at least one photodetector array, each having a plurality of photodetectors which are arranged two-dimensionally in a plurality of rows and in a plurality of columns;

an analog-to-digital converter array having a plurality of analog-to-digital converters which are arranged one-dimensionally such that each analog-to-digital converter corresponds to one row in the at least one photodetector array, each analog-to-digital converter converting, into digital signals, analog signals which are successively outputted from the photodetectors in the corresponding row;

a parallel processing system, including a parallel processing element array and a shift register array, the parallel processing element array having a plurality of processing elements

which are arranged two-dimensionally in a plurality of rows and in a plurality of columns and in one-to-one correspondence with the plurality of photodetectors in the at least one photodetector array, each processing element performing a predetermined calculation on digital signals transferred from the analog-to-digital converter array, the shift register array having a plurality of shift registers which are disposed in one-to-one correspondence with the plurality of analog-to-digital converters and in one-to-one correspondence with the plurality of rows of processing elements, each shift register successively transferring digital signals, which are received from the corresponding analog-to-digital converter and which are equivalent to signals outputted from the photodetectors in a corresponding photodetector row, to predetermined processing elements in the corresponding row; and

a control circuit controlling the photodetector array, the analog-to-digital converter array, the parallel processing system and the shift register array.

However, Patent Claim 1 does not include the following limitations included in App. Claims 1 and 6: a column-direction data-transfer bus including a plurality of column-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of columns in the parallel processing system, each column-direction data-transfer line being connected to the processing elements that are located in the corresponding column and performing data transfer operation with each processing element in the corresponding column; a row-direction data-transfer bus including a plurality of row-direction data-transfer data lines which are arranged in one to one correspondence with the plurality of rows in the parallel processing system, each row-direction data-transfer line being connected to the processing elements that are located in the corresponding row and performing data transfer operation with

each processing element in the corresponding row; and a control circuit performing data transfer operation with the processing elements via the column-direction data-transfer bus and the row-direction data-transfer bus wherein the control circuit controls a combination of data to be transferred via each row data line and column data line to the corresponding processor elements such that each processing element performs a processing that is determined based on the combination of data received from the corresponding row data lines and column data lines.

Furthermore, App. Claims 1 and 6 does include the following limitations included in Patent Claim 1: controlling the shift register array to transfer the digital signals of the next frame to the parallel processing element array, while simultaneously controlling the parallel processing element array to perform the predetermined calculation onto the single frame.

On the other hand, Akerib also disclose a parallel processing system including a control circuit for controlling a column-direction data-transfer bus and a row-direction data-transfer bus while simultaneously processing image data from a single frame while inputting image data from the next frame. More specifically, Akerib discloses, as shown in figures 1 and 3 and as stated in columns 14 (lines 45 – 67), 15 (lines 1 and 2 and 29 – 46), and 18 (lines 4 – 11), a parallel processing system (see figures 1 and 3) including a control circuit (170) for controlling a column-direction data-transfer bus (FIFO Circuit 140) and a row-direction data-transfer bus (registers 180). Additionally, Akerib discloses a parallel processing element array (110) wherein the parallel processing element array (110) has a plurality of processing elements (120 and 122) which are arranged two-dimensionally in a plurality of rows (114) and in a plurality of columns and in one-to-one correspondence with the plurality of photodetectors in the at least one photodetector array (see column 18, lines 4 – 11), each processing element 120 and 122)

performing a predetermined calculation on digital signals transferred from an input array (see column 8, lines 16 – 27), wherein the parallel processing system is controlled to accept the digital signals of the next frame to the parallel processing element array (110), while simultaneously controlling the parallel processing element array to perform the predetermined calculation onto the single frame (see column 14, lines 45 – 60: "FIG. 1 includes a simultaneously accessible FIFO 10, or, more generally, any simultaneously accessible memory, which stores at least a portion of an incoming signal which arrives over a bus termed herein the DBUS. The simultaneously accessible FIFO 10 feeds onto a processor element array 16 including a plurality of PE's 20 which feed onto a datalink 30 which preferably also serves as a responder memory. Each PE 20 stores and processes a subportion of the image, such that the subportions stored and processed by all of the PE's 20 forms the portion of the incoming signal stored at a single time in the simultaneously accessible FIFO 10.")

As stated in columns 66 (lines 56 – 69) and 67 (lines 13 – 15), at the time the invention was made, one with ordinary skill in the art would have been motivated to provide controlling the parallel processing system including the column-direction and row-direction data-transfer buses to accept the digital signals of the next frame to the parallel processing element array, while simultaneously controlling the parallel processing element array to perform the predetermined calculation onto the single frame, as taught by Akerib, to overcome the deficiencies in the App. Claims 1 and 6 and Patent Claim 1, as a means to provide, in an accelerated manner, processing for video and picture editing, as well as camera features such as blur compensation, sharpening, and rotations. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have to overcome the

deficiencies in App. Claims 1 and 6 and Patent Claim 1 by including the simultaneously controlled parallel processing element array taught by Akerib in the Patent Claim 1.

Allowable Subject Matter

9. **Claim 7** is allowed.

10. The following is a statement of reasons for the indication of allowable subject matter.

While the prior art provides a high-speed vision sensor, comprising:

at least one photodetector array, each having a plurality of photodetectors which are arranged two-dimensionally in a plurality of rows and in a plurality of columns;

an analog-to-digital converter array having a plurality of analog-to-digital converters which are arranged one-dimensionally such that each analog-to-digital converter corresponds to one row in the at least one photodetector array, each analog-to-digital converter converting, into digital signals, analog signals which are successively outputted from the photodetectors in the corresponding row;

a parallel processing system, including a parallel processing element array and a shift register array, the parallel processing element array having a plurality of processing elements which are arranged two-dimensionally in a plurality of rows and in a plurality of columns and in one-to-one correspondence with the plurality of photodetectors in the at least one photodetector array, each processing element performing a predetermined calculation on digital signals transferred from the analog-to-digital converter array, the shift register array having a plurality of shift registers which are disposed in one-to-one correspondence with the plurality of analog-to-digital converters and in one-to-one correspondence with the plurality of rows of processing

elements, each shift register successively transferring digital signals, which are received from the corresponding analog-to-digital converter and which are equivalent to signals outputted from the photodetectors in a corresponding photodetector row, to predetermined processing elements in the corresponding row; and

a control circuit controlling the photodetector array, the analog-to-digital converter array, the parallel processing system and the shift register array.

The prior art does not teach or fairly suggest wherein the control circuit receives data from each processing element via both of the corresponding column-direction data-transfer line and the corresponding row-direction data-transfer line and determining the position of a processing element that has outputted predetermined data, based on the combination of a column-direction data-transfer data line that has transferred the predetermined data and a row-direction data transfer data line that has transferred the predetermined data.

11. **Claims 2 – 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter.

As stated above, Parent Claim 1 is rejected under Double Patenting by U.S. Patent 6,608,296 B1 in view of Akerib ('127). However, the prior art does not teach or fairly suggest the limitations as stated in each of Claims 2, 3, 4, and 5, respectively.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is a brief description of each of the cited prior art not used in the rejections as labeled on attached form PTO-892:

- **Prior Art C** discloses, in the very least, a digital image generation device using the parallel processing system of Akerib ('127); however, no details are provided in regards to the image input unit (12) and the analog-to-digital converter means.

- **Prior Art D** discloses, in the very least, an image generation device using a parallel processing system, wherein the parallel processing system comprises a single row of processing elements in one-to-one correspondence with a single row of a two-dimensional photo sensor array. Furthermore, there are no specific details as to whether it is a digital or analog system.

- **Prior Art E** discloses, in the very least, a high data smart image sensor wherein a parallel processing array is comprised of a two-dimensional array of processing elements in one-to-one correspondence with a two-dimensional imager array. However, the system is designed strictly for analog and teaches disadvantages of digital systems.

- **Prior Art F** discloses, in the very least, a two-dimensional amplified array of image sensors, commonly known as APS imagers, wherein a single row of analog-to-digital converters is provided in one-to-one correspondence with a single row of image sensors.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 20, 2004

TUAN HO
PRIMARY EXAMINER